

**REMARKS**

***Summary of the Amendment***

Upon entry of the present Amendment, Claims 31, 34-35, and 44-45 will have been amended. Accordingly, Claims 31-50 are currently pending. By the present Amendment and Remarks, Applicant submits that the rejections have been overcome, and respectfully requests reconsideration of the outstanding Office Action and allowance of the present application.

***Summary of the Office Action***

In the subject Office Action, the Examiner submits that the I.D.S. filed on February 20, 2004 fails to comply with 37 C.F.R. §1.98(a); Claims 34-35 and 44-45 are objected to due to formal matters; Claims 31-36, 38-40 and 48-50 are rejected as being anticipated over the art of record; Claims 41-43 and 46 are allowed; and Claims 37 and 47 are objected to as being dependent upon a rejected base claim, but indicated as being allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

***Acknowledgment of Allowable Subject Matter***

Applicant gratefully acknowledges the Examiner's indication that Claims 41-43 and 46 are allowed. Moreover, Applicant gratefully acknowledges the Examiner's indication that Claims 37 and 47 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

***Information Disclosure Statement***

The Examiner submits that the I.D.S. filed February 20, 2004 fails to comply with 37 C.F.R. §1.98(a)(2), which requires a legible copy of foreign patent. The Examiner submits that the I.D.S. has been placed into the application file but the information referred to therein has not been considered.

Applicant has reviewed the copy of the aforementioned I.D.S. received with the subject Office Action and has the understanding that the only references which were not considered were JP 3177060, JP 1205544, EP 5950939 and EP 5421117. In this regard, each of the remaining references were initialed by the Examiner on October 11, 2004 (as indicated on the copy of the I.D.S. received with the subject Office Action). Therefore, Applicant has submitted replacement copies of JP 3177060, JP 1205544, EP 5950939 and EP 5421117 in a Supplemental I.D.S. filed concurrently herewith.

Thus, Applicant respectfully requests that the Examiner consider the aforementioned references and to indicate the same in the next official Office Action.

***Objection to the Claims***

Claims 34-35 and 44-45 are objected to because in line 2 of each of the claims, “paddle” should be replaced with “pad” according to the Examiner.

As proposed by the Examiner, Applicant has amended Claims 34-35 and 44-45 by deleting the word “paddle” and replacing it with -- pad --. The foregoing amendment is believed to overcome the Examiner’s objection.

***Traversal of Rejections under 35 U.S.C. §102***

***In re HUANG***

Applicant respectfully traverses the rejections of Claims 31-36, 38 and 40 under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,198,171 to Huang et al. [hereinafter “HUANG”].

***A Review of HUANG***

As shown in Figures 3 and 4 of HUANG, a quad flat non-lead semiconductor package 220 is provided. The semiconductor package 220 includes die pad 200, chip 208, leads 202 and molding compound 218. The leads 202 have a first surface 206a and a second surface 206b. A portion of the second surface 206b (bottom surface) excluding a wire-dash bonding protruded zone 226 of the lead 202 is exposed on a second side 202b of the package structure 200 for external connections. The side edge surface 206c of the lead 202 can be exposed to the side edge of the package structure 220. The step structure and the wire-

bonding protruding to zone 226 can be formed by the use of half-etching or coined methods to reduce the thickness of a portion of the lead 202 to increase the encapsulating area of the molding compound onto surfaces of the lead 202.

*Independent Claim 31*

Applicant's independent Claim 31 as amended recites, *inter alia*, . . . an outer lead portion, *a portion of the first surface defined by the outer lead portion being sized and configured for electrical connection to a conductive terminal*; . . . Applicant submits that HUANG does not teach the aforementioned features.

As discussed above, a portion of the second surface 206b (bottom surface) of each of the HUANG leads 202 is exposed on the second side 222b of the semiconductor package 200 for external connections. It is noted that the first surface 206a is substantially encapsulated by the molding compound 218. It is evident from the disclosure in HUANG that the only manner contemplated to connect the semiconductor package 220 to any other electrical terminals is via second surfaces 206b of the leads 202. Furthermore, it is evident that the small portion of the first surface 206a which is not encapsulated by molding compound 218 is not adapted to be attached to any sort of electrical terminal.

On the other hand, the present invention provides an outer lead portion 32 that is not encapsulated and projects outwardly from the side surface 24c of the body 24. Moreover, a portion of the first surface 28a of the lead 28 defined by the outer lead portion 32 is sized and configured for electrical connection to a conductive terminal. Therefore, HUANG differs from the present invention recited in independent Claim 31 because the first surface 206a of the HUANG lead 202 is not adapted or intended to be connected to a conductive terminal. Hence, HUANG does not anticipate the invention recited in independent Claim 31 since HUANG does not teach, *inter alia*, an outer lead portion, a portion of the first surface defined by the outer lead portion being sized and configured for electrical connection to a conductive terminal.

For the foregoing reasons, and because HUANG fails to disclose the above-noted features of the present invention, Applicant submits that HUANG fails to disclose each and every feature of the present invention as recited in independent Claim 31.

Accordingly, Applicant submits that the Examiner has failed to provide an adequate evidentiary basis to support a rejection under 35 U.S.C. §102(e) and that the present rejection of Claim 31 is improper and should be withdrawn.

*Dependent Claims 32-36, 38 and 40*

Applicant further submits that dependent Claims 32-36, 38 and 40 are allowable at least for the reason that these claims depend from allowable independent Claim 31 and because dependent Claims 32-36, 38 and 40 recite additional features that further define the present invention.

Accordingly, Applicant requests that the Examiner reconsider and withdraw the rejection of dependent Claims 32-36, 38 and 40 under 35 U.S.C. §102(e) and indicate that these claims are allowable.

*In re SHARMA*

Applicant respectfully traverses the rejection of Claims 31 and 38-39 under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,420,779 to Sharma et al. [hereinafter “SHARMA”].

*A Review of SHARMA*

Figure 1 of SHARMA provides a cross-sectional illustration of a semiconductor package 100 which includes integrated circuit chip 110, die pad 120, leads 130 and 140, and molding compound 150. Leads 130 each include a top surface 131 and a bottom surface 132. Leads 140 each include a top surface 141 and a bottom surface 142. Further, it is noted that a small portion 133 of the top surface 131 of each lead 130 is not encapsulated. Similarly, a small portion of the top surface 141 of each lead 140 is not encapsulated. Molding compound 150 encapsulates chip 110, die pad 120 and leads 130 and 140 such that bottom surface 122 of the die pad 120 and bottom surfaces 132, 142 of the leads 130, 140 are coplanar with bottom surface 152 of molding compound 150. Therefore, bottom surfaces 122, 132 and 142 of die pad 120, leads 130 and leads 140, respectively, are exposed such that they can be electrically connected to a printed circuit board.

*Independent Claim 31*

Applicant's independent Claim 31 as amended recites, *inter alia*, . . . an outer lead portion, *a portion of the first surface defined by the outer lead portion being sized and configured for electrical connection to a conductive terminal*; . . . Applicant submits that SHARMA does not teach the aforementioned features.

As discussed above, the bottom surfaces 132, 142 of the SHARMA leads 130, 140 are exposed in the bottom surface 152 of the molding compound 150 for external connections. On the other hand, the top surfaces 131, 141 are substantially encapsulated by the molding compound 150. It is evident from the disclosure in SHARMA that the only manner contemplated to connect the semiconductor package 100 to any other electrical terminals is via the bottom surfaces 132, 142 of the leads 130, 140. Furthermore, it is evident that the small portions of the top surfaces 131, 141 of the leads 130, 140 which are not encapsulated by molding compound 150 are not adapted to be attached to any sort of electrical terminal.

On the other hand, the present invention provides an outer lead portion 32 that is not encapsulated and projects outwardly from the side surface 24c of the body 24. Moreover, a portion of the first surface 28a of the lead 28 defined by the outer lead portion 32 is sized and configured for electrical connection to a conductive terminal. Therefore, SHARMA differs from the present invention recited in independent Claim 31 because the top surfaces 131, 141 of the SHARMA leads 130, 140 are not adapted or intended to be connected to a conductive terminal. Hence, SHARMA does not anticipate the invention recited in independent Claim 31 since SHARMA does not teach, *inter alia*, an outer lead portion, a portion of the first surface defined by the outer lead portion being sized and configured for electrical connection to a conductive terminal.

For the foregoing reasons, and because SHARMA fails to disclose the above-noted features of the present invention, Applicant submits that SHARMA fails to disclose each and every feature of the present invention as recited in independent Claim 31.

Accordingly, Applicant submits that the Examiner has failed to provide an adequate evidentiary basis to support a rejection under 35 U.S.C. §102(e) and that the present rejection of Claim 31 is improper and should be withdrawn.

*Dependent Claims 38 and 39*

Applicant further submits that dependent Claims 38 and 39 are allowable at least for the reason that these claims depend from allowable independent Claim 31 and because dependent Claims 38 and 39 recite additional features that further define the present invention.

Accordingly, Applicant requests that the Examiner reconsider and withdraw the rejection of dependent Claims 38-39 under 35 U.S.C. §102(e) and indicate that these claims are allowable.

*In re BERG*

Applicant respectfully traverses the rejection of Claims 48-50 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,756,380 to Berg et al. [hereinafter “BERG”].

*A Review of BERG*

Figure 2 of BERG shows a cross-section of plastic ball grid array (PBGA) package 100. The package 100 includes an organic substrate 110 having various conductive layers, typically formed from copper, which has been laminated to the substrate and etched into a desired pattern. A copper layer is used to form a plurality of conductive traces 112 on both a top surface and bottom surface of the substrate 110. On the top surface, conductive traces 112 are used to establish electrical connection to the semiconductor die 102 which is mounted onto the substrate 110. The conductive traces 112 on the top surface are routed to corresponding conductive traces 112 on the bottom surface through a plurality of conductive vias 114. The substrate 110 further includes a die pad 116 which is the area of the substrate 110 on which semiconductor die 102 is mounted with the use of die attach material 108. Die pad 116 is made from the same conductive layer used to form conductive traces 112. A permanent masking layer 128 is selectively positioned on both the top surface and bottom surface of substrate 110. On the top surface, resist mask 128 preferably covers the entire surface other than those portions of conductive traces 112 which are plated with the plating layers 126. Plating of the conductive traces on the bottom surface of substrate 110 is

performed to enable subsequent attachment of solder balls 132 which are positioned in an array configuration.

*Independent Claim 48*

Applicant's independent Claim 48, recites, *inter alia*, . . . *a substrate having opposed first and second surfaces . . . a die pad disposed on the first surface of the substrate . . . a plurality of circuit patterns disposed on the first surface of the substrate . . . a semiconductor chip attached to the die pad . . . the outer end portion of each of the circuit patterns is exposed outside of the package body to serve as an input/output terminal.* Applicant submits that BERG does not teach the aforementioned features.

As stated above, the BERG invention mounts a semiconductor die 102 to a substrate 110 to form a PBGA package 100. Even though portions of the substrate 110 extend beyond the encapsulant 130, there is no circuit patterns formed on the top surface thereof intended to serve as input/output terminals. Indeed, BERG teaches that those portions of the conductive traces 112 which are disposed on the top surface of the substrate 110 outside of the package body 130 and not covered by the plating layers 126 are completely covered by the resist mask 128. Accordingly, the portions of the conductive traces 112 residing on the top surface of the substrate 110 along with the die pad 116 and not covered by the package body 130 are incapable of functioning as input/output terminals. Therefore, Applicant respectfully submits that BERG does not teach, *inter alia*, . . . *a plurality of circuit patterns disposed on the first [top] surface of the substrate [wherein] the outer end portion of each of the circuit patterns is exposed outside the package body to serve as an input/output terminal.*

Since BERG fails to disclose the above-noted features of the present invention, Applicant submits that BERG fails to disclose each and every feature of the present invention as recited in independent Claim 48.

Accordingly, Applicant submits that the Examiner has failed to provide an adequate evidentiary basis to support a rejection of anticipation under 35 U.S.C. §102(b) and that the rejection of independent Claim 48 is improper and should be withdrawn.

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*Dependent Claims 49-50*

Further, Applicant submits that dependent Claims 49-50 are allowable at least for the reason that these claims depend from allowable independent Claim 48 and because these claims recite additional features that further define the present invention.

Accordingly, Applicant requests that the Examiner reconsider and withdraw the rejection of dependent Claims 49-50 under 35 U.S.C. §102(b) and indicate that these claims are allowable.

**CONCLUSION**

In view of the foregoing, it is submitted that none of the references of record, when considered either alone or in any proper combination thereof anticipate or render obvious Applicant's invention as recited in Claims 31-40, 44-45 and 47-50. The applied references of record have been discussed and distinguished while significant claimed features of the present invention have been pointed out.

Applicant respectfully submits that each and every pending claim of the present application meets the requirements for patentability under 35 U.S.C. §§ 112, 102 and 103. Accordingly, allowance of the present application of all the claims therein is respectfully requested and believed to be appropriate.

Further, any amendments to the claims which have been made in this response and which have not been noted to overcome a rejection based upon the prior art, should be considered to have been for a purpose unrelated to patentability, and no estoppel should be deemed to attach thereto.

If any additional fee is required, please charge Deposit Account Number 19-4330.

Respectfully submitted,

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